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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,299	11/27/2001	Woon-kyung Lee	4591-222	9003

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MARGER JOHNSON & MCCOLLOM PC
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER
VU, DAVID

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,299	LEE, WOON-KYUNG	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Paterson et al.,(US 4,697,330).

In re claims 1,3 and 8, Paterson et al, in related text (Col. 8, Lines. 1-68) and figures (Figs. 1-8) disclose a method of fabricating a flash memory device having a cell array region and a peripheral circuit region, the method comprising: forming a device isolation layer20 at a predetermined region of a semiconductor substrate10 to define at least one first active region in the cell array region and a second active region in the peripheral circuit region; forming a floating gate pattern26 covering the first active region and a gate conductive layer38/40 covering the peripheral circuit region; sequentially forming an inter-gate dielectric layer28/30 and a control gate conductive layer38 on an entire surface of the substrate having the floating gate pattern26 and the gate conductive layer38; and selectively removing the control gate conductive layer38 and the inter-gate dielectric layer28/30 which are located in the peripheral circuit region, thereby exposing the gate conductive layer38/40 in the peripheral circuit region.

In re claim 2, further comprising: forming a tunnel oxide layer interposed between the floating gate pattern and the first active region; and forming a gate oxide layer interposed between the gate conductive layer and the second active region (Figs. 2-3)

In re claim 4, in which the floating gate pattern and the gate conductive layer are formed of a doped polysilicon layer (Col. 8, Lines. 36-37)

In re claim 5, in which the doped polysilicon layer is formed using an ion implantation technique (Col. 8, Lines. 47-48).

In re claim 6, in which the ion implantation technique is performed using boron as dopants (Col. 8, Lines. 47-48).

In re claim 7, in which the doped polysilicon layer is formed using $POCl_3$ as a dopant source (Col. 8, Lines. 36-37).

In re claim 9, further comprising: forming a metal silicide layer on the control gate conductive layer in the cell array region and the exposed gate conductive layer in the peripheral circuit region (Fig. 6a)

In re claim 10, further comprising: patterning the metal silicide layer, the control gate conductive layer, the inter-gate dielectric layer and the floating gate pattern that are located in the cell array region, thereby forming a word line crossing over the first active region and a floating gate interposed between the word line and the first active region; and patterning the metal silicide layer and the gate conductive layer that are located in the peripheral circuit region, thereby forming a gate electrode crossing over the second active region. (Fig. 7)

In re claim 11, further comprising: patterning the control gate conductive layer, the inter-gate dielectric layer and the floating gate pattern that are located in the cell array region, thereby

forming a word line crossing over the first active region and a floating gate interposed between the word line and the first active region; and patterning the gate conductive layer that are located in the peripheral circuit region, thereby forming a gate electrode crossing over the second active region. (Figs. 7&8a,b,c)

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm.
If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

PV
David Vu

Art Unit 2818

HOAI HO
PRIMARY EXAMINER